REMARKS

This Preliminary Amendment amends the above identified Utility Patent Application filed herewith. With this Preliminary Amendment, claims 1-16 have been cancelled. Claims 17-39 have been added. Claims 17-39 remain pending in the application and are presented for consideration and allowance.

A substitute specification is included herewith. The specification contains no new matter.

Preliminary Amendment
Applicant: Nicola Da Dalt
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Title: DEVICE AND METHOD FOR FREQUENCY SYNTHESIS

CONCLUSION

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 500471.

Any inquiry regarding this Preliminary Amendment should be directed to Steven E. Dicke at the below-listed telephone numbers.

The Examiner is invited to contact the Applicants' representative at the below-listed telephone number to facilitate prosecution of this application.

Respectfully submitted,

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313.1450.

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~~Description~~

DEVICE AND METHOD FOR FREQUENCY SYNTHESIS

Field of the Invention

The present invention relates to a device and a method for frequency synthesis, particularly for frequency synthesis with the use of digitally controlled oscillators.

Background

Oscillators capable of generating only certain frequencies are frequently used in semiconductor electronics. An example of such oscillators are digitally controlled oscillators (DCOs). Such a digitally controlled oscillator is represented exemplarily in Figure 1. In this figure, the digitally controlled oscillator 1 is supplied with a parameter s_{in} which can assume only a finite number of discrete values. The parameter can be any physical quantity, such as current, voltage, capacitance, inductance, resistance and the like. The value that is assumed by this parameter is usually determined by the status (value) of a digital bus. In the following, the various possible values of the digital bus are designated as digital words, and denoted by D1,D2, ..., DN. The set of all digital words is designated as S(D) = {D1, D2, ..., DN}. An output frequency of the output signal f_{OUT} of the digitally controlled oscillator 1 is uniquely assigned to a specific value of the input parameter s_{in}, i.e., to a specific digital word out of the set S(D). It follows from this that the digitally controlled oscillator can generate only a discrete set of output frequencies. In the following, these frequencies are denoted by f1, f2, ..., fN, and the corresponding set of all possible frequencies is denoted by S(f). It is assumed that the frequency fi is assigned to the digital word Di.

In many applications, it may be the case that a frequency which is not included in the set S(f) is to be generated by the digitally controlled oscillator. An example of this is a closed-loop control circuit, in which the output frequency of the digitally controlled oscillator is to be regulated to a multiple of a certain reference frequency, for example through use of a phase-locked loop (PLL). This reference frequency or its multiples is/are generally independent of the frequencies that can be generated by the digitally controlled oscillator, and therefore generally does not/do not correspond with elements of the set S(f).

Hitherto, this problem has been solved by techniques which usually make extensive use of analog circuits. An example of this is N-frequency-divider synthesis, used for wireless data transmission. In this synthesis, an oscillator, in this case a voltage-controlled oscillator, is driven by analog control signals. The desired output frequency is generated, in that an N-frequency divider is used in the feedback path of the frequency synthesis device. Usually in this case, the module of the N-frequency divider is digitally controlled by a higher-order (≥ 2) delta-sigma modulator, in order to reduce disturbing components of the output spectrum of the synthesis device. This solution, however, requires the use of analog circuits, with the typical problems associated with same. An example of this are variations in the gain due to variations in power, voltage or temperature. Moreover, this solution cannot be directly transferred to digital frequency synthesis architectures, in which there is no feedback path.

Summary

~~It is therefore the object of t~~The present invention ~~to~~ provides a device and a method by ~~means of which~~ a frequency synthesis that is as accurate as possible can be realized with a small amount of resource and, in particular, the use of a digital control is possible.

~~This object is achieved by a device according to claim 1 and by a method according to claim 12. The sub-claims define preferred or advantageous exemplary embodiments of the invention.~~

According to the invention it is proposed that oscillator ~~means~~ system that can be driven for the purpose of generating, out of a set of at least two possible output frequencies, an output frequency that can be picked off at an output, be so driven that, for the purpose of generating a desired frequency that is not included in the set of possible output frequencies, the oscillator means alternately generates at least two different output frequencies, out of the set of possible output frequencies, in such a way that the average value of the generated output frequencies over a time period is substantially the desired frequency.

The at least two generated output frequencies are in this case preferably alternated at an average frequency that is greater than the reciprocal value of the time period over which the average value is formed. The oscillator means in this case may comprise a digitally controlled oscillator, or may consist of same. However, it is also conceivable, for example, for the oscillator means to consist of a plurality of individual oscillators which respectively generate only a single frequency.

In this case, the frequency at which the alternation of the at least two output frequencies is performed is substantially dependent on the output frequencies. In particular – in the case of exploitation of averaging effects – it may be selected to be less than the at least two output frequencies or, also, greater than the latter.

The oscillator ~~means~~system, or the digitally controlled oscillator, may in this case comprise, for example, a ring oscillator to which a current, out of a set of possible currents, is supplied for the purpose of driving the oscillator. Alternatively, or additionally, there may be an LC element through which the

output frequency can be determined. In this case, the LC element may comprise one or more switchable capacitors, with the result that the total capacitance of the LC element can be varied and the output frequency can thus be controlled. Alternatively, the capacitance of the LC element may include one or more varactor diodes, through the driving of which the total capacitance of the LC element may be varied. In addition, the device may comprise one or more frequency dividers connected to the output of the oscillator means.

Brief Description of the Drawings

~~The invention is explained more fully in the following with reference to the appended drawing and a preferred exemplary embodiment. In the drawing:~~

The accompanying drawings are included to provide a further understanding of the present invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain the principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated, as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

Figure 1 ~~shows~~illustrates the principle of a digitally controlled oscillator~~;~~.

Figure 2 ~~shows~~illustrates the digitally controlled oscillator from Figure 1~~;~~ with a driving means~~;~~.

Figure 3 ~~shows~~illustrates a linear model of a digitally controlled oscillator~~;~~.

Figure 4 ~~shows~~illustrates ~~a possible~~one embodiment of a digitally controlled oscillator~~;~~.

Figure 5 ~~shows~~illustrates a second ~~possible~~ embodiment of a digitally controlled oscillator~~;~~.

Figure 6 ~~shows~~illustrates a third ~~possible~~ embodiment of a digitally controlled oscillator~~;~~.

Figure 7 ~~shows~~illustrates a block diagram of a device, according to the invention, for realizing circuit simulations~~, and~~.

Figures 8a-8c ~~show~~illustrate simulated signal characteristics of the circuit represented in Figure 7.

Brief Description

Figure 1 ~~shows~~illustrates, as explained in detail at the outset, the principle of a digitally controlled oscillator 1.

In Figure 2, compared with Figure 1, there is additionally a control device 2 for driving the digitally controlled oscillator 1. The control device may be, for example, a digital processor which drives the digitally controlled oscillator 1 via a digital control bus. A digital control signal s_{in} is sent to the digitally controlled oscillator 1 via the digital control bus. This digital control signal s_{in} can assume values, for example current values, voltage values or resistance values, out of a finite set of possible input signals S(D). In dependence on the control signal s_{in}, the digitally controlled oscillator 1 generates an output signal f_{OUT}, the frequency of which is in each case uniquely assigned to a certain control signal s_{in} out of the set S(D). From this it is evident that the output frequency likewise originates from a finite set S(f) of possible output frequencies.

If it is then necessary or desired to generate an output signal f_{OUT} at a frequency that is not included in the set S(f), according to the invention the control device 2 drives the digitally controlled oscillator 1 such that the latter

generates at least two different frequencies, out of the set S(f), so that the time average of the frequency of the output signal f_{OUT} results in exactly this desired frequency.

The time averaging in this case is effected over a time period T_{av}. The value of T_{av} depends on the respective application. The least possible value for T_{av} is one period of the output clock pulse of the digitally controlled oscillator.

A digitally controlled oscillator, controlled by a single-bit bus by which the two values of the control signal s_{in}, namely D1=0 and D2=1, can be transmitted, may serve in this case as a simplified example of a device according to the invention. The digitally controlled oscillator can thus be driven to output only two frequencies, namely f1 and f2. If it is then desired to generate a frequency that is exactly between these two frequencies f1 and f2, namely (f1+f2)/2, this can be realized in that the control signal s_{in} alternates with a pulse duty factor of 50% between the values D1 and D2.

In general, a desired frequency can also be generated by averaging over more than two frequencies, in that the control signal s_{in} alternates between the corresponding values out of the set S(D).

In order to obtain a correct output frequency, an average switch-over frequency f_s between the various necessary control signals s_{in} out of the set S(D) must be greater than the inverse of the averaging time period T_{av}. How much greater, depends on how rapidly the output signal f_{OUT} of the digitally controlled oscillator reacts to changes of the control signal s_{in}.

This lag can be understood by reference to the linear model of a digitally controlled oscillator represented in Figure 3. In the case of this model, the control signal s_{in} is first supplied to a low-pass filter 3, which produces a filtered control signal s_{filt} from the control signal s_{in}. In the linear model, it is taken as a basis that the frequency of the output signal f_{OUT} is to be a linear function of the

filtered input signal s_{filt}. Accordingly, as represented in simplified form, the linear oscillator multiplies the signal s_{filt} by a constant K, in order to obtain an intermediate signal f_k having an intermediate frequency. In order to obtain the output signal f_{OUT}, there is added to the frequency of the intermediate signal f_k a further signal f_0, which corresponds to the frequency of the digitally controlled oscillator when the control signal s_{in} is equal to zero.

The lag of the digitally controlled oscillator depends in this case on the cut-off frequency of the low-pass filter. A small cut-off frequency means a long lag, or a large intrinsic averaging effect, of the digitally controlled oscillator.

If the averaging time period T_{av} is only one period of the output clock pulse of the digitally controlled oscillator (no averaging), the value of s_{in} must be changed several times during the time T_{av} ($f_s >> 1/T_{av}$). In this case, f_s is thus greater than f1 and f2 of the digitally controlled oscillator. If the reaction of the digitally controlled oscillator is sufficiently slow, f_s can be reduced by reason of the intrinsic averaging effect of the digitally controlled oscillator and, in this case – if necessary, with the exploitation of averaging effects of downstream frequency dividers – also become smaller, or substantially smaller, than the frequencies f1 and f2, this permitting simpler driving at high frequencies. If the intrinsic averaging effect of the digitally controlled oscillator is particularly great, it is also possible to use as a control signal s_{in} a bit stream that has been generated according to the delta-sigma principle and, if necessary, noise-shaped. The high-frequency noise produced in this case is removed by the low-pass filter before the output signal f_{OUT} is generated.

Various realization possibilities for the digitally controlled oscillator are to be explained in the following.

Figure 4 ~~shows~~illustrates an exemplary embodiment of a digitally controlled oscillator based on a ring oscillator. In this case, the actual ring oscillator consists of transistors T and resistors R as a chain of series-connected

inverters. The frequency of the ring oscillator in this case is determined by the current that flows through the transistors T of the ring oscillator. This current is determined by a current source I0 and by current sources I1-I4 that can be switched by switches S1-S4. The thus determined total current is transferred to the ring oscillator through the current mirror circuit M1-M4. The thus designed oscillator is digitally driven in this case by opening and closing of the switches S1-S4. Closing of the switches S1-S4 causes the respective current I1-I4 to be added to the minimum current I0.

A further possibility is to use an LC oscillatory circuit as a digitally controlled oscillator. In this case, the oscillation frequency is determined by the values of the inductance L and of the total capacitance C. In this case, the value $1/\left(2\pi \text{ x } \sqrt{LC}\right)$ is obtained, in a first approximation, as an output frequency. In this case, the output frequency can be digitally controlled through variation of the total capacitance C. If C can assume only a finite number of discrete values, the output frequency of the digitally controlled oscillator can assume only a discrete number of values.

A first example of this is represented in Figure 5. In the case of the oscillator represented in Figure 5, the total capacitance C is formed by the capacitors C1-C7. In this case, the capacitors C1-C6 can be switched by switches S5-S10. The total capacitance can thus be varied through actuation of the switches. The inductance L in this case remains fixed. In addition, there is a driving circuit 6, which is supplied with a fixed current I_{bias}. This driving current serves to compensate losses that occur in the oscillatory circuit. The output signal can then be picked off at the terminations denoted by f_{OUT} or $f_{OUT,Q}$.

A similar oscillator is represented in Figure 6. Instead of the capacitors from Figure 5, here there are varactor diodes V1-V3, the capacitance of which can be controlled by a voltage applied to the terminations b_0-b_2. Thus, again, it is possible to adjust the total capacitance and to control the output frequency of

the oscillator. In other respects, the structure of the oscillator represented in Figure 6 is identical to that represented in Figure 5. The advantage of the circuit represented in Figure 6 compared with that represented in Figure 5 is that no switches are required.

A digitally controlled oscillator similar to that represented in Figure 6 was used to perform simulations. The structure used for simulation is represented schematically in Figure 7.

A oscillator 1 is used which is based on an LC oscillatory circuit and digitally controlled by a single-bit control signal s_{in}. The digitally controlled oscillator can generate only two frequencies: 2.1 GHz and 2.18 GHz. The output frequency is first divided by six by a first frequency divider 7, and then again divided by four by a second frequency divider 8, so that in total the frequency is divided by 24. Accordingly, overall, the two frequencies 87.5 MHz and 90.8MHz can be generated by means of the arrangement. A frequency of 89.2 MHz, which is exactly between these two frequencies, is then to be generated using this arrangement. This can be achieved in that the control bit is switched over between the two states, with a pulse duty factor of 50%. In the simulation represented in the following, the switch-over time was two nanoseconds. The switch-over frequency f_s = 1/2ns = 500 MHz is thus substantially less than the frequencies that are generated by the digitally controlled oscillator.

Figure 8 ~~shows~~illustrates the results of the simulation. Figure 8a ~~shows~~illustrates the time characteristic of the voltage of the control signal and the time characteristic of the frequency and of the voltage of the signal f_{OUT} generated by the digitally controlled oscillator. Figures 8b and 8c respectively show the time characteristic of the frequency and of the voltage of the signal after the first and the second frequency divider respectively. As shown in Figure 8c, the output frequency fluctuates by only a small amount around the desired value of 89.2 MHz. The relative frequency error at the output of the digitally controlled oscillator is 3.7%. The frequency dividers cause the averaging period

to be extended. At the output of the second frequency divider, the relative frequency error is still only 0.22%. An even smaller frequency error can be achieved through a shorter switch-over time. Exploitation of the averaging effects of the frequency dividers 7, 8, however, enables a good result to be achieved, even with a switch-over time which is long compared with the output frequencies of the digitally controlled oscillator. Obviously, a similar result might also be achieved with an oscillator which – as already described – has a large intrinsic averaging.

It is thus demonstrated that, by means of a device according to the invention and a method according to the invention, it is possible to generate an output frequency which does not directly correspond to a frequency that can be generated by the oscillator used.